Principal Digital Design Engineer

INNOPHASE is a rapidly growing communications semiconductor startup with headquarters located in San Diego, CA. We are developing complete wireless solutions with significantly improved power dissipation/performance tradeoffs as compared to industry competitors. Our innovative technology also dramatically improves wireless product flexibility and ease-of-use for product developers. We are looking for driven candidates to join our fast-paced and motivated team.

In this job you will be working with a team of digital design engineers to develop novel SoC products for connectivity and communications. You will also be a key contributor to product definition and resulting detailed device performance and functional requirements specifications. In addition to delivering high quality digital solutions in the context of the product architecture, the team supports other disciplines with work product such as Veriloga stimulus files, test benches for device bringup/characterization, test vectors for product manufacturing, etc.

Key Responsibilities

- Contribute to/review SoC specifications and architectures
- Front to back digital design and verification – RTL through physical implementation
- Hands on technical leadership
- Support schedule and resource planning
- Help define and socialize digital/system design, implementation methodologies and test strategies and flows
- Debug designs and provide timely closure
- Work with System, Software, RF, Analog, and Test teams and provide necessary support

Desirable Skills

- Experience with Cadence F2B design tools
- Experience with formal verification tools
- Able to work effectively with incomplete or changing requirements
- Good skills an interest in mentorship
- Strong knowledge of mixed signal concepts
- Focused, goal driven finisher

Job Requirements

- Experience bringing highly integrated mixed signal SoCs to commercial mass production
- Experience with embedded systems, wireless protocols, power management, signal processing and standard digital interfaces
- Deep knowledge of Verilog and SystemVerilog
- Deep knowledge of front-end tools (Verilog simulators, linters, clock-domain crossing checkers)
- Proven knowledge of synthesis, static timing, DFT and (Front to Back) F2B digital SoC design flow
- Experience with ATPG, fault grading, scan, BIST, DFT/DFM
- Proven knowledge of SystemVerilog assertions, checkers, and other design verification techniques
- Knowledge of languages such as C/C++, Perl, Tcl and Python
- Strong communication and presentation skills
- Good skills and interest in mentorship
- Ability to foresee issues and design in flexibility and workarounds for both known and unknown unknowns
- Team player with strong sense of urgency to complete projects on time

10+ years experience digital SoC Development required

MS/PhD EE/CS preferred.