Digital Design Sr. Manager/Director

INNOPHASE is a rapidly growing communications semiconductor start-up with headquarters located in San Diego, CA. We are developing complete wireless solutions with significantly improved power dissipation/performance tradeoffs as compared to industry competitors. Our innovative technology also dramatically improves wireless product flexibility and ease-of-use for product developers. We are looking for driven candidates to join our fast-paced and motivated team.

In this job you will be responsible for leading a team of digital SoC development engineers to create novel/game changing products for connectivity and communications applications. You will also be a key contributor to product definition and resulting detailed device performance and functional requirements specifications. Your team will deliver high quality digital solutions in the context of the product architecture, integration of in-house digital and mixed signal IP, drive the selection and integration of purchased IP, as well as support other teams with work product such as Veriloga stimulus files, test benches for device bring-up/characterization, test vectors for product manufacturing, etc.

Key Responsibilities

- SoC development, leadership, and ownership
- Hands on digital SoC (ASIC) team leadership
- Work with Marketing, Systems Engineering, Verification, Firmware, RF/Analog, and Test teams to successfully develop complex SoC products
- Hiring, organization development, resource planning, scheduling, performance management as well as overall team execution
- Establish digital/system architectures and design, implementation methodologies and test strategies as well as develop and define flows and tools. Debug designs and provide timely closure of issues

Desirable Skills

- Experience developing highly integrated mixed signal SoCs including wireless communications
- Experience with embedded systems, wireless protocols, power management, signal processing and standard interfaces (I2C, SPI, UART, etc.)
- Experience with Cadence F2B design tools
- Experience with formal verification and DFT/ATPG/BIST tools
- Proven knowledge of System Verilog assertions, checkers, and other design verification techniques

Job Requirements

- Proven track record of leading multiple complex SoCs from concept to mass production
- Expert in RTL design and implementation (architecture and micro-architecture)
- Deep knowledge of front-end tools and flow - Verilog simulators, linters, synthesis, static timing, clock trees, power simulation, floor plan development, and power supply implementation
- Deep knowledge of system modeling and verification using System Verilog or System C
- Proven knowledge in acquiring and integrating 3rd party IP
- High speed logic design (GHz+) , and high speed clock distribution experience.
- Knowledge of coding and scripting languages such as C/C++, Python.
- Understanding of mixed signal concepts
- Strong communication and presentation skills
- Strong technical leadership skills
- Strong team builder and recruiter
- Ability to distill key requirements from incomplete inputs
- Ability to foresee issues and design in flexibility and workarounds for both known and unknowns
- Team player with strong sense of urgency to complete projects on time

10+ years' experience managing digital design teams required. MS/PhD EE/CS preferred.