Principal SOC Verification Design Engineer

INNOPHASE is a rapidly growing ultralow-power wireless semiconductor startup with headquarters located in San Diego, CA. We are developing complete wireless solutions with significantly differentiated power dissipation/performance tradeoffs. Our innovative technology also dramatically improves wireless product flexibility and ease-of-use for product developers. We are looking for driven candidates to join our fast-paced and motivated team to drive excellence in our 5G products. his role is an excellent opportunity for someone that enjoys a small and agile group where you can make a great impact.

The Principal SOC Verification Design Engineer is a full-time position based in San Diego. In addition to benefits and perks below, Innophase offers relocation assistance!

Key Responsibilities

- Construct IP, SoC level test benches using verification components developed at the IP level. Test bench architecture for random/directed testing, stimulus generation, and checking to include custom and off the shelf VIP/UVCs.
- Develop and execute SoC verification plans focused on IP block interoperability and SOC/System level. Develop and execute verification plans based on design specifications and collaboration with architects and designers.
- Construct HW/SW Co-Verification
- Be part of a dynamic and functionally diverse team with opportunities for gaining exposure to modeling (TLM), HW emulation/acceleration, and SW driven verification.
- Utilize constrained random verification, functional coverage, code coverage and assertions to achieve goals.

Benefits and Perks

- Competitive salary and stock options
- Learning and development opportunities
- Employer paid health benefits
- Paid vacation/holidays/sick/parental leave
- Flexibility to balance quality work and personal lives
- Annual holiday and summer events
- Free snacks and drinks

Job Requirements

- Master's degree in engineering (or equivalent).
- 10+ years of experience in design verification - Proven experience in full chip verification from test plan development to tape-out sign-off.
- Experience constructing chip-level System Verilog and UVM test bench environments, writing System Verilog Assertions (SVAs), with embedded software design and test.
- Experience executing block or chip-level verification plans.
- Experience with HW/SW Co-Verification - Developing test benches, test cases/use-cases, APIs, their execution, and debug.
- Excellent debug skills, with experience debugging RTL in block and/or chip-level environments.
- Extensive experience with a variety of verification tools and environments, and a deep understanding of their differences and capabilities to optimize the right methodology with schedules as the top priority.
- Experienced in SystemVerilog, UVM, and scripting languages like Python and Tcl.
- Expertise in using industry standard simulation tools such as NC Verilog, VCS, QuestaSim, etc.
- Excellent communication skills, energetic and self-motivated.

APPLY NOW!

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